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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/707,842	01/16/2004	Haining S. Yang	FIS920030238	1841

29625 7590 04/22/2005

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EXAMINER	
LINDSAY JR, WALTER LEE	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 04/22/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/707,842	YANG ET AL.	
	Examiner	Art Unit	
	Walter L. Lindsay, Jr.	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *17-19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/16/2004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to an Election filed on 1/28/2005.

Currently, claims 1-19 are pending. Claims 20-24 have been cancelled.

Election/Restrictions

1. Applicant's election without traverse of claims 1-19 in the reply filed on 1/28/2005 is acknowledged.

Specification

2. The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

3. Claims 18 and 19 are objected to because of the following informalities: in claim 18, "4.5 x 109 dynes/cm2" should be "4.5x 10^9 dynes/cm^{2}" and in claim 19, "5.5 x 109 dynes/cm2" should be "5.5x 10^9 dynes/cm^{2}". Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 5 and 7 are rejected under 35 U.S.C. 102(b) as being anticipated by Doshi et al. (U.S. Patent No. 6,277,720 dated 8/21/2001).

Doshi shows the method as claimed in Figs. 1-11 and corresponding text as: depositing a nitride film (30) along a surface (col. 8, lines 8-22) of the substrate (2) and the gate stack (10) (col. 7, lines 51-65), wherein the nitride film is thicker over a surface of the substrate and thinner over a portion of the gate stack (col. 8, lines 8-22) (claim 1). Doshi teaches that the nitride film is non-conformal nitride film (col. 8, lines 8-22) (claim 5). Doshi teaches that the deposition of the nitride film provides enhanced stress within a transistor channel (col. 8, lines 8-22) (claim 7).

6. Claims 8-14 are rejected under 35 U.S.C. 102(b) as being anticipated by Becker (U.S. Patent No. 6,153,501 dated 11/28/2000).

Becker shows the method as claimed in Figs. 5 and 6 and corresponding text as: depositing a layer of nitride film (62A) over a gate stack (52A, will represent the stack) and a surface of a substrate (50) (col. 2, lines 44-62); removing the nitride film on the gate stack to provide enhanced stress in a transistor channel under the gate stack (col. 3, lines 8-16) (claim 8). Becker teaches that a resist material (64) is deposited on a surface of the nitride film over the substrate while leaving a surface of the nitride film proximate an upper portion of the gate stack (col. 3, lines 8-16) (claim 9). Becker teaches the removal of an upper portion of the gate stack and the nitride film disposed thereon (col. 3, lines 17-25) (claim 10). Becker teaches that depositing the resist comprises depositing one of a spin-on material, an anti-reflection coating, an oxide film, and a low k material (col. 3, lines 8-16) (claim 11). Becker teaches that spacers are formed at a lower portion of the sidewalls of the gate stack (col. 3, lines 8-16) (claim 12). Becker teaches that the spacers are formed includes forming the spacers along

substantially all of the sidewall and etching the spacers to form spacers at the lower portion of the sidewalls (col. 3, lines 8-16) (claim 13). Becker teaches that depositing a resist comprises depositing at least one of an oxide layer or a borophosphorsilicate glass on low spots and leaving high spots exposed (col. 3, lines 8-16) (claim 14).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

9. Claims 2-4 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Doshi et al. (U.S. Patent No. 6,277,720 dated 8/21/2001) in view of Pan et al. (U.S. Patent No. 6,198,144 dated 3/6/2001).

Doshi shows the method substantially as claimed in the preceding paragraph.

Doshi lacks anticipation only in not explicitly teaching that: 1) a spacer is formed adjacent only a lower portion of the gate stack (claim 2); 2) forming the spacer comprises reducing a size of the spacer (claim 3); 3) reducing the spacer comprises

reactive ion etching (claim 4); and 4) depositing the nitride film comprises a plasma enhanced vapor deposition process (claim 6)

Pan shows the formation of spacers that only cover lower portions of the gate stack and that a nitride film is deposited by (PECVD). Layer 20 is formed over the substrate and gate stack and is then etched to form spacers covering only a lower portion of the gate stack (col. 5, lines 21-32). Layer 22 is then formed over the substrate and gate stack, this layer is formed by PECVD, it can then be reduced and etch by reactive ion etching techniques (col. 5, lines 33-51). The advantages of these techniques aids in providing thicker portions on the horizontal portions (substrate) and thinner on vertical surfaces (gate stack) (col. 2, lines 54-64). Another advantage is the fact that the nitride film reduces the conversion of conductive layers into non – conductive layers (col. 3, lines 16-32).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Doshi by forming a spacer along the lower portions and forming a nitride by PECVD, as taught by Pan with the motivation that Pan teaches that thicker portions of deposited layers are formed on horizontal portions while thinner portions are formed on vertical portions and the nitride film reduces the conversion of conductive layers into non-conductive layers.

10. Claims 15 and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Becker (U.S. Patent No. 6,153,501 dated 11/28/2000) in view of Pan et al. (U.S. Patent No. 6,198,144 dated 3/6/2001).

Becker shows the method substantially as claimed in the preceding paragraph.

Becker lacks anticipation only in not explicitly teaching that: 1) removing a portion of the gate stack and the nitride film disposed thereon comprises reactive ion etching (claim 15); and 2) removing a portion of the gate stack and the nitride film disposed thereon comprises chemical mechanical polishing (claim 16).

Pan shows the formation of spacers that only cover lower portions of the gate stack and that a nitride film is deposited by (PECVD). Layer 22 is then formed over the substrate and gate stack, this layer is formed by PECVD, it can then be reduced and etch by reactive ion etching techniques (col. 5, lines 33-51). The advantages of these techniques aids in providing thicker portions on the horizontal portions (substrate) and thinner on vertical surfaces (gate stack) (col. 2, lines 54-64). Another advantage is the fact that the nitride film reduces the conversion of conductive layers into non – conductive layers (col. 3, lines 16-32). Chemical mechanical polishing is well known and often used in etching nitride films.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to modify the method of Becker by etching a nitride film by reactive ion etching and chemical mechanical polishing, as taught by Pan with the motivation that Pan teaches that thicker portions of deposited layers are formed on horizontal portions while thinner portions are formed on vertical portions and the nitride film reduces the conversion of conductive layers into non-conductive layers.

Allowable Subject Matter

11. Claims 17-19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: the prior art, either singly or in combination fails to anticipate or render obvious, the limitations of:

...further comprising forming spacer adjacent a sidewall of the gate stack and etching upper portions of the spacer to form sidewalls **only** at a lower portion of the sidewalls, as required by claim 17 as it depends on claim 8;

...wherein the gate is about 60 nm wide, a spacer is about 50 nm wide, and the nitride film provides a stress of about 2.Gpa, the enhanced stress in the transistor channel is greater than approximately 4.5×10^9 dynes/cm^2 at about 5nm below a gate oxide, as required by claim 18, as it depends from claim 8; and

...wherein for a semiconductor device having a gate about 60 nm wide, a spacer about 50 nm wide, and a nitride film stress of about 2.0Gpa, the enhanced stress in the transistor channel is greater than approximately 5.5×10^9 dynes/cm^2 at about 5 nm below a gate oxide, as required by claim 19, as it depends from claim 8.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Walter L. Lindsay, Jr. whose telephone number is (571) 272-1674. The examiner can normally be reached on Monday-Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael S. Lebentritt can be reached on (571) 272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Walter L. Lindsay, Jr.
Examiner
Art Unit 2812

WLL
April 14, 2005